REMARKS

The disclosure is objected to because of the following informalities – Throughout the application, there are words that are not separated by spaces, such as in [0002], line 1, "systemfor" or [0017], lines 2-3 "comprisesa" Furthermore, there are other typos such as two consecutive commas in [0013], line 11.

All missing spaces between words found by the applicant and also the double comma problem of paragraph [0013] indicated by the Examiner are corrected. No new matter is entered. Withdrawal of the objection to the disclosure is respectfully requested.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The title is amended to read, "METHOD FOR EXECUTING PATCH PROGRAM SEGMENTS AND MICROPROCESSOR APPARATUS THEREOF". No new matter is entered. Applicant points out that the new title is clearly indicative of the invention to which the claims are directed. In particular, claim 3 is a method for executing patch program segments and claim 1 is a microprocessor apparatus. Withdrawal of the objection to the title is respectfully requested.

Claims 1-3 are objected to because of the following informalities. b. "afirst," claim 1 should be "a first." c. "aninitializing," claim 1, should be "an initializing." d. "storingthe," claim 2, should be "storing the." e. "comparinga," claim 3, should be "comparaing a." f. "aninitializing," claim 3, should be "an initializing."

In additional to the claim amendments described in more detail below, all missing spaces between words indicated by the Examiner in the claims are corrected. No new matter is entered. Withdrawal of the objection to claims 1-3 is respectfully requested.

Claims 1-5 are rejected under 35 USC 112, second paragraph, as being indefinite for

failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The reasons are that:
Claim 3 recites the limitation "the table entry" in the last line but there is insufficient antecedent basis. Claims 4 and 5 are rejected for failing to alleviate the rejections of claim 3 above.

Claim 3 is amended to change "the table entry" to "an entry in the table" to correct the antecedent basis problem found by the Examiner. No new matter is entered.

Claim 4 recites the limitation "the patch" in line 2 but there is insufficient antecedent basis for this limitation as it may differ from "patch program segments" of claim 3, line 1.

Claim 4 is amended to change "the patch" to "a finished patch program segment" to correct the antecedent basis problem found by the Examiner. No new matter is entered.

Claim 5 recites the limitation "the read only memory" in lines 2-3 but there is insufficient antecedent basis for this limitation in the claim.

Claim 5 is amended to firstly include the limitation "wherein the first program is stored in a read only memory", which introduces and thereby provides antecedent basis for "the read only memory". No new matter is entered.

In claim 1, the applicant should insert indentations and lines between the paragraphs designating the components of the apparatus in order to better convey the components of this apparatus. It is indefinite as to where in the apparatus the read only memory, the auxiliary programmable-memory, and the controller lie.

Applicant has added indentations and lines between the paragraph designating the components of the apparatus of claim 1 in order to better convey the components as requested by the Examiner. Additionally, applicant has moved the final wherein clause of claim 1 (last part of original claim 1) to be its own paragraph (now last paragraph of claim 1) also

separated from the preceding claim element by a blank line for clarity. No new matter is entered.

Claims 1-5 are rejected under 35 USC 102b as being anticipated by Hagqvist et al (US 5581776).

Applicant has amended claim 1 to include the feature that "the processing unit is for executing the indirect branch instruction to thereby insert the replacement program count value corresponding to the match into the program counter." (emphasis added) No new matter is entered. For instance, see paragraph [0041] of the invention stating, "The processing unit 54 will then execute the indirect branch instruction by using the attached index to search the table of replacement count values. Upon location of the proper table entry, the processing unit 54 will replace the program count value currently loaded in the program counter 56 with the replacement count value given by the table entry."

Applicant notes that such operation is in contrast to the teachings of Hagqvist. In particular, Hagqvist do not teach the CPU 10 executing an indirect branch instruction to thereby change the program counter. Instead, Hagqvist teach that the program counter is loaded without involvement of the CPU 10 at all (i.e, the program counter is loaded using program counter load controller 26 after getting a match by the address comparator 22). Afterwards, the CPU 10 will therefore be directed to a new address for executing subsequent instructions. For example, see col 3, lines 32-35 of Hagqvist stating, "As a result, address comparator 22 issues a control signal to program counter load controller 26 which causes a program count of 301 to be written from branch control register 24 into program counter 28. CPU 10 then responds to program count 301..."

In the rejection of original claim 1, the Examiner stated (see Office action dated 03/12/2007) that this so-called branch process that does not involve the CPU 10 as taught by Hagqvist is interpreted by the Examiner to fall within the scope of "an indirect branch instruction" because "this replacement of the program counter constitutes an indirect branch instruction, as the microprocessor is indirectly instructed to branch without a branch

instruction actually being decoded" (see OA dated 03/12/2007)

However, applicant points out that the indirect branch instruction of the invention is in fact executed by the processing unit. In this way, in the invention, no program counter load controller is needed to insert the replacement program count value into the program counter. Additionally, as explained in paragraph [0049], reduced hardware and cost are direct results of the processing unit itself executing the indirect branch instruction to thereby insert the replacement program count value into the program counter according to the invention.

Therefore, applicant asserts that currently amended claim 1 should be found allowable with respect to the teachings of Hagqvist for at least the reason that Hagqvist do not teach that "the processing unit is for executing the indirect branch instruction to thereby insert the replacement program count value corresponding to the match into the program counter", as is claimed in claim 1. Claim 2 is dependent upon claim 1 and should therefore be allowable for at least the same reason.

Concerning independent claim 3, amendments similar to the above described for claim 1 are made. In particular, claim 3 is amended to include the steps executing the indirect branch instruction by the processing unit to thereby access a table in programmable memory according to the index of the indirect branch instruction, and changing the program count value of the program counter by the processing unit according to an entry in the table as a result of executing the indirect branch instruction. (emphasis added)

Similar to claim 1, applicant asserts that currently amended claim 3 should be found allowable with respect to the teachings of Hagqvist for at least the reasons that Hagqvist does not teach that the processing unit is for executing the indirect branch instruction to thereby access a table in the auxiliary programmable memory according to the index of the indirect branch instruction, and also does not teach changing the program count value of the program counter by the processing unit according to an entry in the table as a result of executing the indirect branch instruction. As explained above, the CPU 10 of Hagqvist is not involved in

any part of the branching from loading the program counter 28 with the new address value. Claims 4 and 5 are dependent upon claim 3 and should therefore be allowable for at least the same reasons.

Reconsideration and allowance of claims 1-5 with respect to the above remarks is respectfully requested.

Conclusion:

Thus, all pending claims are submitted to be in condition for allowance with respect to the cited art for at least the reasons presented above. The Examiner is encouraged to telephone the undersigned if there are informalities that can be resolved in a phone conversation, or if the Examiner has any ideas or suggestions for further advancing the prosecution of this case.

Sincerely yours,

Winston Hsu Date: 06.11.2007

Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)